In the Claims

The following listing of the claims replaces all previous listings.

1. (Currently Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

~~determining~~ providing a power supply capacitor cell in combination with a corresponding logic gate cell so that a capacitance value of the power supply capacitor ~~cells so as to correspond~~ cell corresponds to a drive load capacity value of the logic gate ~~cells~~ cell, and

arranging the power supply capacitor ~~cells~~ cell in a vicinity of the logic gate ~~cells~~ cell so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply ~~cells~~ capacitor cell.

C1

2. (Currently Amended) The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor ~~cells~~ cell is determined to be substantially twice as large as the drive load capacity value of the logic gate ~~cells~~ cell.

3. (Currently Amended) The LSI layout method according to claim 1, wherein the power supply capacitor ~~cells are~~ cell is arranged in the vicinity of the logic gate ~~cells~~ cell which ~~change~~ changes simultaneously with clock synchronization.

4. (Currently Amended) A LSI layout method ~~for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells,~~ according to claim 1, further comprising the operations of:

calculating a possible number of the power supply capacitor cells to be arranged based on a width of a dead space of the power supply and a width of the power supply capacitor cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.

5. (New) The LSI layout method according to claim 1, wherein the power supply capacitance cell includes:

a p-sub wafer;

a n-well fixed to the ground line on the p-sub wafer, and

a polysilicon gate fixed to the power supply line on the n-well.

6. (New) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells; comprising the operations of:

providing a power supply capacitor cell in combination with a corresponding logic gate cell so that a capacitance value of the power supply capacitor cell corresponds to a drive load capacity value of the logic gate cell, and

arranging the power supply capacitor cell adjacent to the logic gate cell so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.